AN X-BAND 10 W MONOLITHIC TRANSMIT-RECEIVE GaAs FET SWITCH

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ABSTRACT

A monolithic transmit-receive GaAs FET switch capable of switching more than 10 W CW power with about 1 dB insertion loss and 26 dB isolation at X-band frequencies is reported.

INTRODUCTION

The use of FETs as microwave switches has been reported earlier [1]-[5]. In this paper we will describe the use of such FET switches in a microwave power switching application. We will describe the design, fabrication and performance of a MMIC X-band 10 W transmit-receive GaAs FET switch.

DESIGN CONSIDERATIONS

The basic FET switch element, in shunt mode of operation is shown in Fig. 1a. The FET switch is a three-terminal device with the gate voltage V_G controlling the switch states. In a typical switch mode, the high impedance state (switch closed) corresponds to a negative gate bias larger in magnitude than the pinchoff voltage ($|V_g|>|V_p|$), and the low impedance state (switch open) corresponds to zero gate bias. These two linear operation regions of the FET are shown schematically in Fig. 1b. Note that in either state virtually no dc bias power is required.

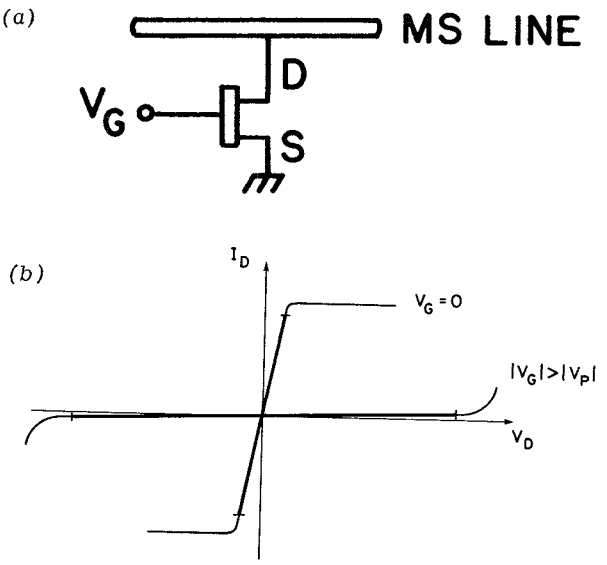

Figure 1. (a) Basic GaAs switch in shunt mode of operation; (b) Switch FET linear operating regions.

The small signal equivalent circuit for the two states of the switch for a unit 1 mm gate periphery device can be represented as shown in Fig. 2.

Note that these values are dependent on the channel geometry, channel doping and pinchoff voltage of the device. Also note that, unlike the PIN diode, the total capacitor shunting the high impedance R_H represents a reactance of the order of 50 ohms at X-band frequencies. Therefore, to realize the switching action, this capacitance must either be resonated or its effect must be included in the design of the impedance matching sections.

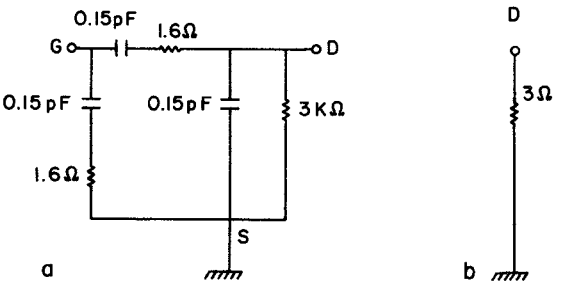

Figure 2. Approximate equivalent circuit used in the designs for a switch FET. (a) High resistance state; (b) Low resistance state.

For microwave power switching using FETs, there are additional considerations. One of these considerations is the maximum allowable rf voltage swing across the device. The variation of the rf

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voltage on the drain and gate terminals with respect to the grounded source is shown in Fig. 3 for one period.

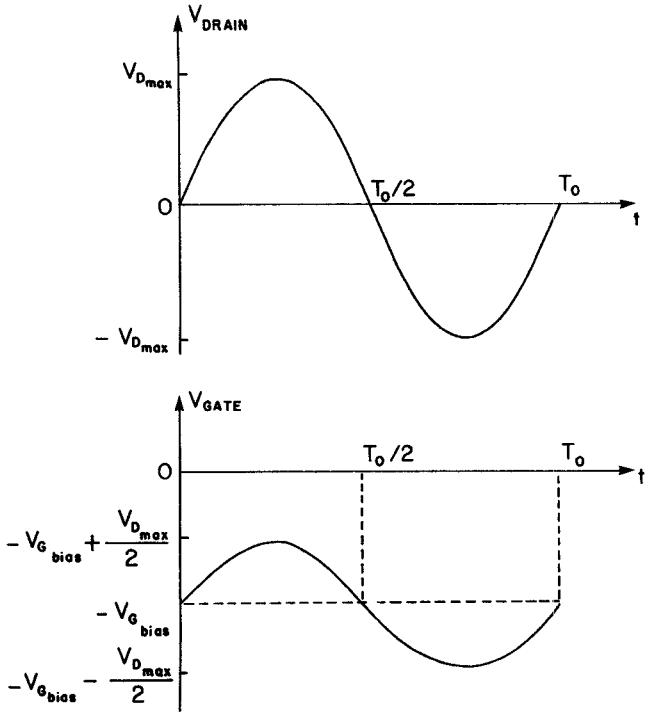

Figure 3. Variation of the large signal rf voltages on drain and gate terminals, over one period.

In this figure, it is assumed that the gate terminal of the switch FET is rf open. This condition should be realized in the design of the gate bias circuitry.

Under the above assumption and due to the fact that gate-to-drain impedance and gate-to-source impedance is equal (see the equivalent circuit in Fig. 2), half of the drain voltage swing appears in the gate terminal, as it is illustrated in Fig. 3 Constraints on the terminal voltages can be summarized as follows. During the first half of the period, the total gate voltage should not fall below the pinchoff voltage V_p. During the entire cycle, the difference between the drain and gate voltages should not exceed the gate-drain breakdown voltage. These constraints can mathematically be expressed as

$$-V_{G_{bias}} + \frac{V_{Dmax}}{2} = -V_p \qquad (1)$$

$$V_{dmax} + V_{G_{bias}} - \frac{V_{dmax}}{2} = V_B \qquad (2)$$

From the above two equations, the maximum allowable drain voltage and the required gate bias condition can be solved as

$$V_{d_{max}} = V_B - V_p \qquad (3)$$

and

$$V_{G_{bias}} = \frac{V_B - V_p}{2} \qquad (4)$$

Hence, if the impedance level that the switch FET sits in its high impedance state is Z_o, then the maximum power that can be transmitted in the switch closed position can be calculated as

$$P_{max} = \frac{1}{2} \frac{(V_B - V_p)^2}{Z_o} \qquad (5)$$

Using the notation of the schematic TR-switch shown in Fig. 4, Z_o can approximately be calculated by transferring the 50 ohm antenna terminal impedance through the quarter wavelength MS line of characteristic impedance Z_1, as

$$Z_o \simeq \frac{Z_1^2}{50} \qquad (6)$$

Hence, Eq. (5) can be rewritten as

$$P_{max} = 25 \frac{(V_B - V_p)^2}{Z_1^2} \qquad (7)$$

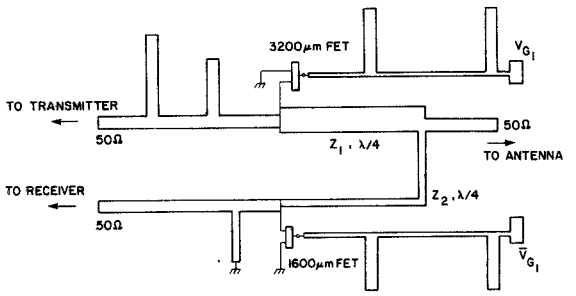

Figure 4. Schematic circuit diagram of the 10 W transmit-receive switch.

The maximum power calculation under switch closed condition is relevant to the transmitter arm of a transmit-receive (TR) switch. For the receiver arm, the constraints are different. During the time when the transmitter power is on, the switch on the receiver arm is in the open state. In this low impedance condition, it should be able to sustain essentially the short circuited current in the receive arm due to the transmitter pulse. Again using the notation of Fig. 4, peak value of this current can be calculated as

$$I_{max}\Big|_{\text{switch open}} = 20\sqrt{\frac{P_{Transmitted_{max}}}{Z_2(50 + Z_2)}} \quad . \quad (8)$$

Equations (7) and (8) fully specify the constraints on the switch FETs under power switching conditions. First note that constraints on the transmitter and the receiver arm switches are completely independent. Also note that in Equation (5), periphery of the device is not a parameter. Thus, once Z_1 is chosen from power requirements, the device periphery on the transmitter arm can be determined purely from small signal insertion loss analysis. Equation (8) on the other hand does bring in the device periphery as a design parameter for the receiver arm switch since the maximum current that a device can support in its linear region before it reaches the saturation is directly proportional to its gate periphery. The characteristic impedance of the receiver arm, Z_2, also enters into the equation. It is easy to see that, by increasing Z_2, one can meet the requirement of Eq. (8) readily.

CIRCUIT DESCRIPTION

The schematic circuit diagram of the switch is shown in Fig. 4. The switch is fabricated on 0.1 mm GaAs substrate. A photograph of the finished chip is shown in Fig. 5. The chip dimensions are 4.5 × 3.7 mm. In the transmit arm, a single-gate, interdigitated 3.2 mm total gate periphery FET is used. The receive arm uses a single-gate FET of 1.6 mm total periphery.

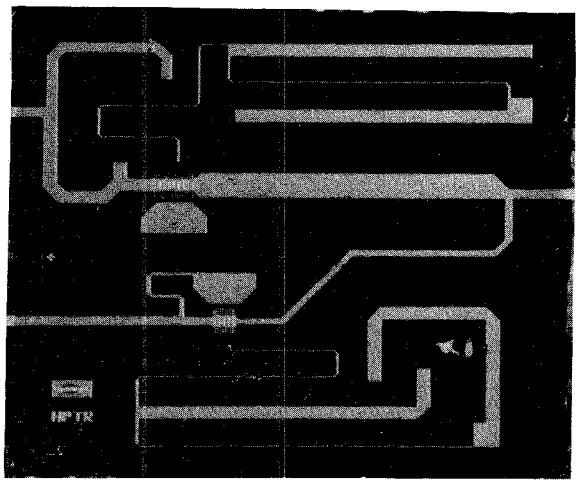

Figure 5. Finished chip.

The dc gate circuitry is provided monolithically on-chip. It is essentially a low pass filter which provides high impedance to the gate of the device and isolates the bias pad at the edge of the chip from rf leakage, at X-band frequencies.

FABRICATION TECHNOLOGY

Circuits are processed on vapor phase epitaxy layers grown by the $AsCl_3$ system on semi-insulating GaAs substrates. The three layer structures consist of a high-doped contact layer ($n > 2 \times 10^{18}$ cm^{-3}, $t = 0.2$ μm), on active layer of low doping ($n = 5 \times 10^{16}$ cm^{-3}, $t = 0.6$ μm), and an undoped buffer region ($n < 5 \times 10^{13}$ cm^{-3}, $t = 2$ μm). Device isolation is achieved with a combination of a shallow mesa etch and a damaging 160^+ implant.

Ohmic contacts are formed by alloying the standard Ni/AuGe metallization into the surface. The gates, which are recessed, consist of a Ti/Pt/Au (1000/1000/3000 Å) metalization and are nominally 1 μm long.

The transmission line structures and air-bridge interconnects are gold plated to 4 μm thick. Via-holes are etched through the wafer to ground points on the frontside.

THE EXPERIMENTAL PERFORMANCE

The high power TR switch is characterized in the measurement jig shown in Fig. 6. Experimental data for the small signal insertion loss for both transmit and receive arms and the isolation of the receiver is presented in Fig. 7. The insertion loss is around 0.8 dB for the transmitter and 1.6 dB for the receiver arm. Isolation is higher than 25 dB. Input and output return loss is better than 10 dB in 8.5 to 10.5 GHz frequency range.

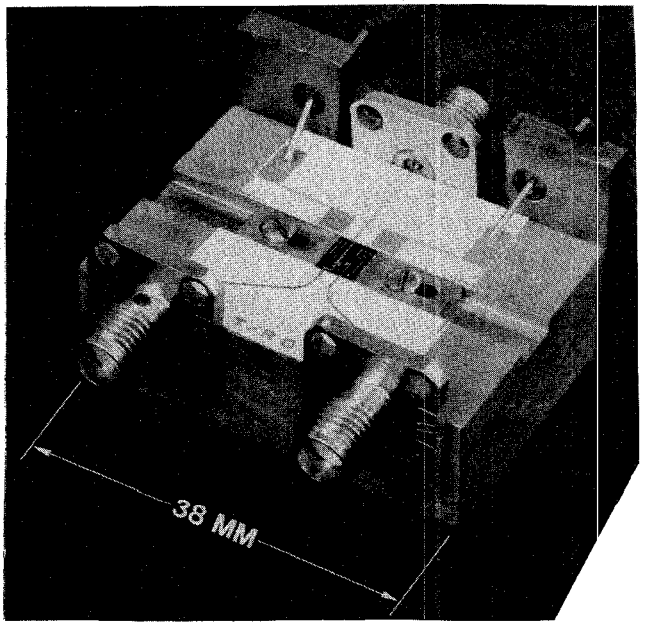

Figure 6. Measurement jig.

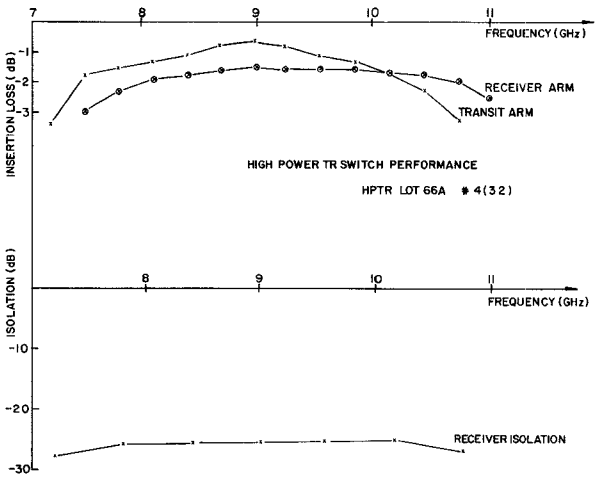

Figure 7. Small signal TR switch performance.

The predicted insertion loss and isolation performance of the circuit is presented in Fig. 8. The difference between the predicted and the experimental insertion loss and isolation performance can be explained in terms of the higher than predicted low field resistances that were obtained with the switch FETs.

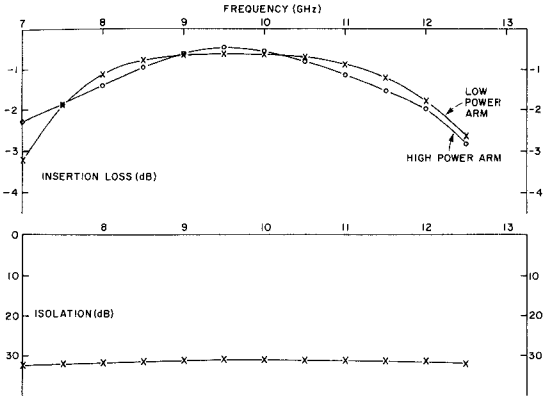

Figure 8. Predicted performance of the switch circuit.

Large signal insertion loss performance is shown in Fig. 9, and the isolation performance is shown in Fig. 10 for up to 10 W input power at center frequency. No degradation from small signal performance is observed up to 10 W of CW microwave power.

CONCLUSION

A monolithic transmit-receive GaAs FET switch capable of switching more than 10 W CW rf power is reported. The small signal insertion loss of the SPDT switch is about 1 dB in the 8-10 GHz frequency range. The isolation between the transmit and receive arms is better than 25 dB. No degradation in insertion loss or isolation is observed for input powers up to 10 W. No drain bias is employed in the FETs and the only dc power dissipation is that due to the gate leakage current.

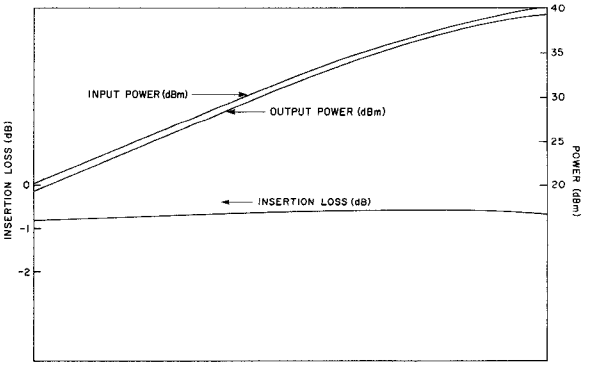

Figure 9. Large signal insertion loss performance.

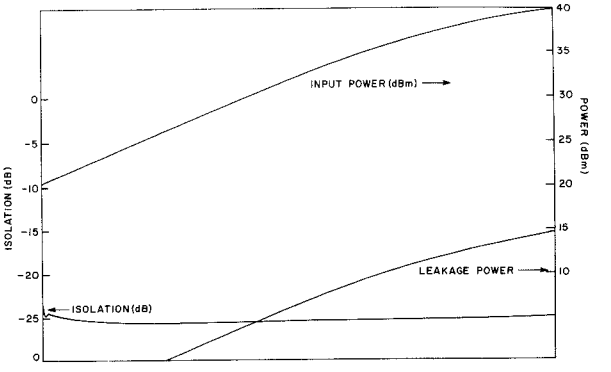

Figure 10. Large signal isolation performance.

The demonstrated power levels, negligible dc power requirement and subnanosecond switching times [4] make these monolithic switches attractive for future phase array radar systems.

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